Digital Logic Scope Tutorial for the BA31XX Labs

Supplement

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Introduction to Mixed Signal Oscilloscope (MSO)

The MSO-X-3024A is the third generation Mixed Signal Oscilloscope (MSO) from Agilent. This model has advanced triggering features and updated display features. Otherwise that is it is equivalent to the older Agilent model. Figure 1 shows the user interface
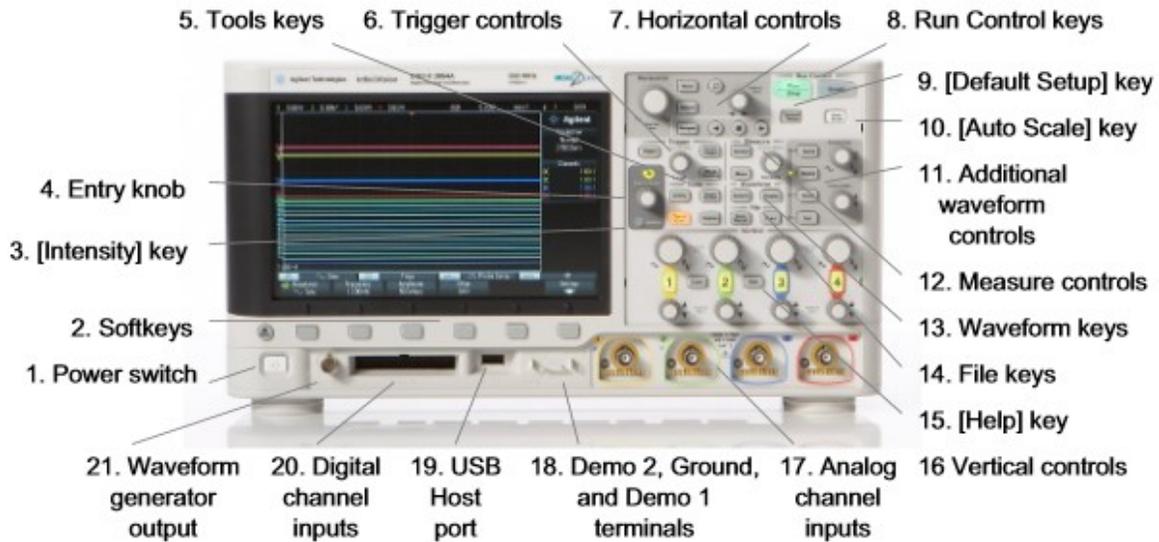

Figure 1

For the purpose of this DESL lab, you will only worry about the following interfaces

Digital channel inputs (20), **Trigger controls (6)**, **Soft Keys (2)** and **Tool keys (5)** as shown in figure 1.

The first thing you need to do is ask the TA to get the digital logic cable probes out of the black cabinets. Connect the 40 pin header to the digital channel inputs as shown in figure 2.
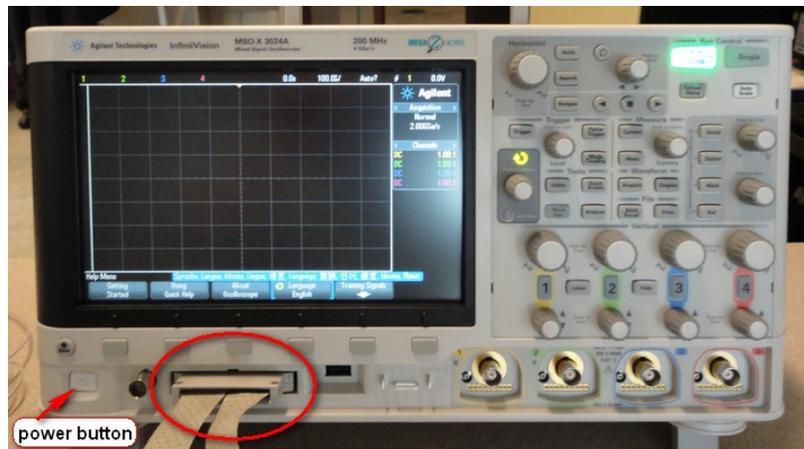
After the 40 pin header has been attached turn the **Power** button on. See figure 2 for location of the power button.

Viewing a Signal

To view a signal, there are three main steps that you must take.

- Turn on your digital signals and turn off the analog signals on the MSO.
- Output the signals you want to view onto an output pin on the board.
- Attach a probe to the output pin you assigned your signal to.

Viewing signals on MSO

Follow these steps to ensure you have the proper signal display on the MSO. As mentioned earlier we will be concentrating on the digital channels as opposed to the analog channels. Turn off all analog control buttons **1**, **2**, **3** and **4**. See figure 3 for their location on front panel. If any of the buttons are highlighted press them until they are off. This should ensure none of the analog channels will be displayed on the display screen.
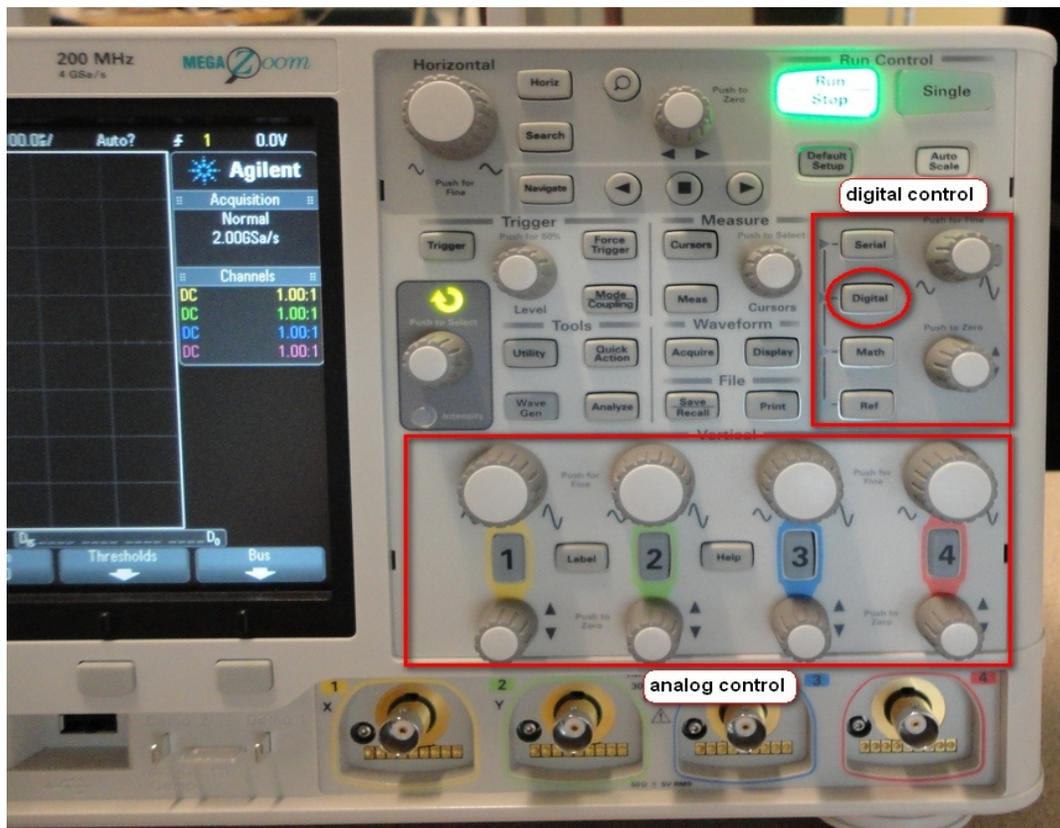

Figure 3

Press the **digital** button found in the digital control section of the front panel. It is circled in figure 3. This will display all the digital channels on the screen. Notice the six buttons just below the display. They have the following characteristics.

Button 1- **Scale size**. Depending on the number of channels that are displayed you can increase or decrease the vertical size of the signal. For all 15 channels you will need to use the medium or small scale. IF you use the large scale then only 8 channels can be displayed. Press the button several times and you will get the following results. See figure 4a, 4b and 4c for examples of results when selecting the different scale modes.
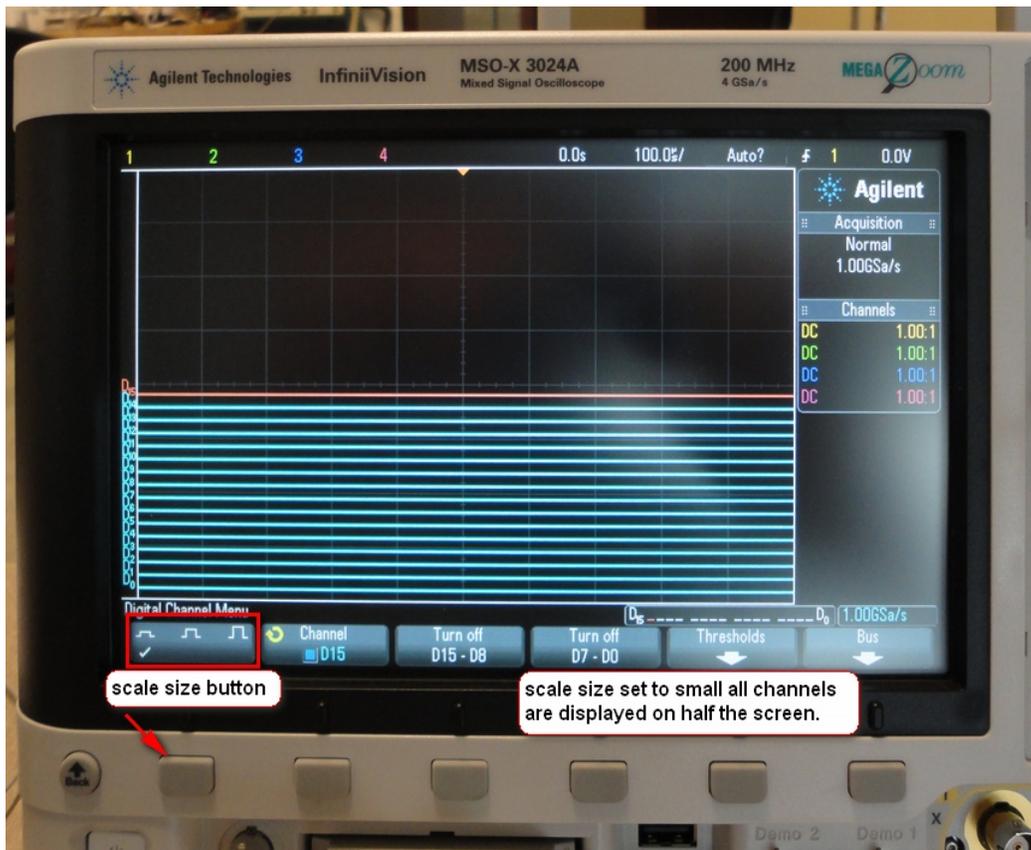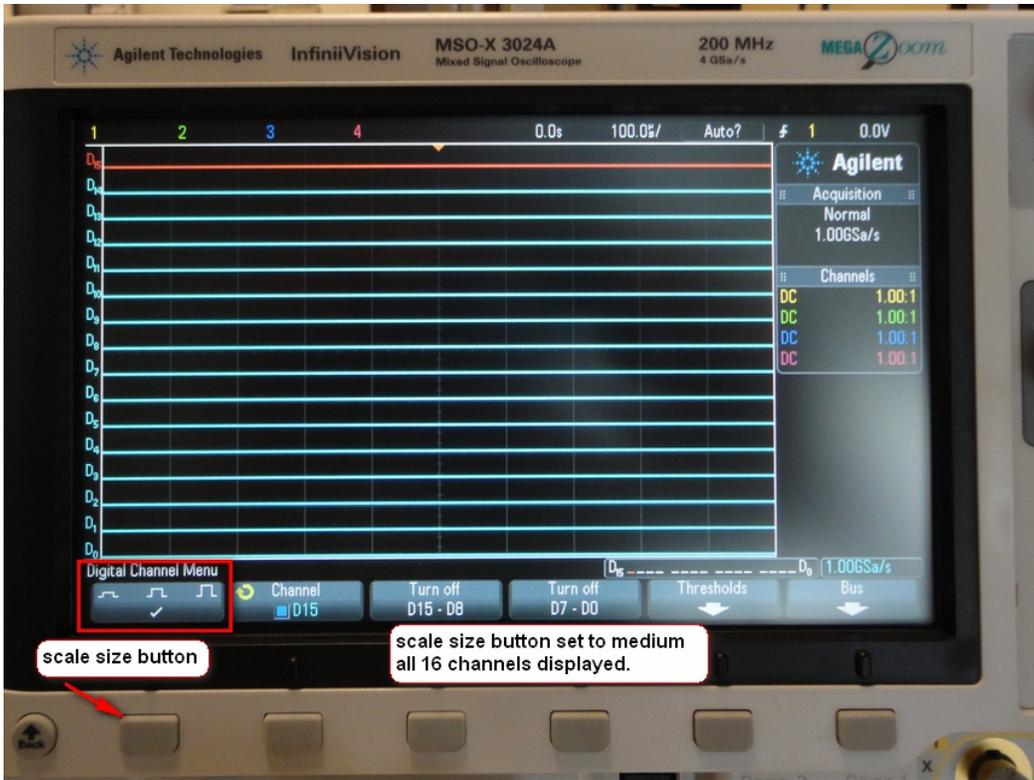

Figure 4a- small scale setting.

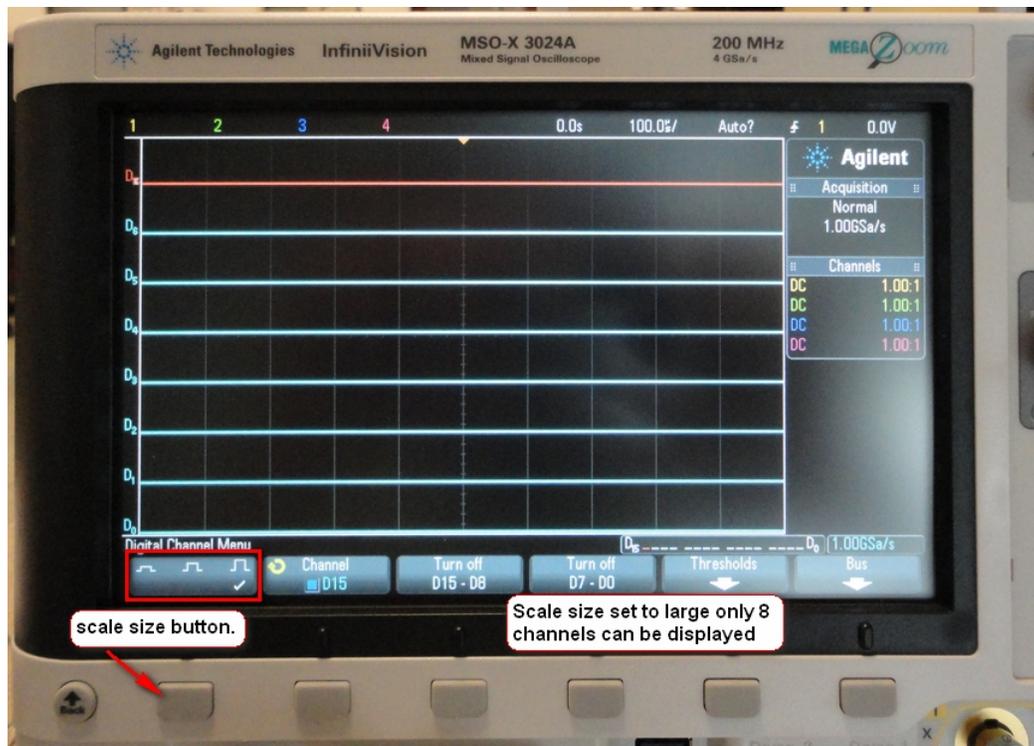Figure 4b- medium scale setting.

Figure 4c- large scale setting.

Button 2- Individual **channel** select. This button allows you to select any channel from 0 to 15. The channel that is selected will be highlighted red on the display. By pressing the **select** knob the channel will be removed or displayed on the screen. See figure 5
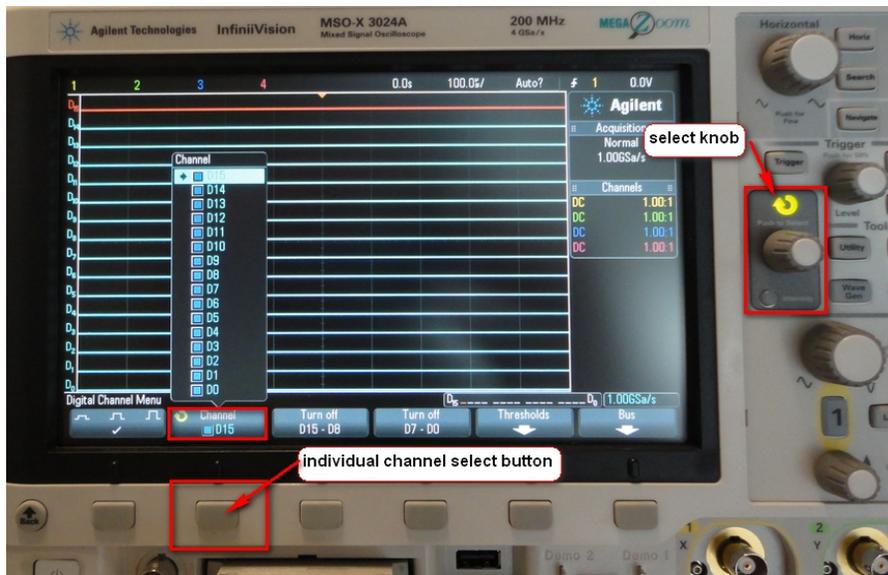

Figure 5- In this case channel 15 is selected. By pressing the select knob the channel can be removed or displayed.

Button 3- **Channel 15 – 8** select. This button is used to select or remove channels 15 down to 8 as a group. See figure 6
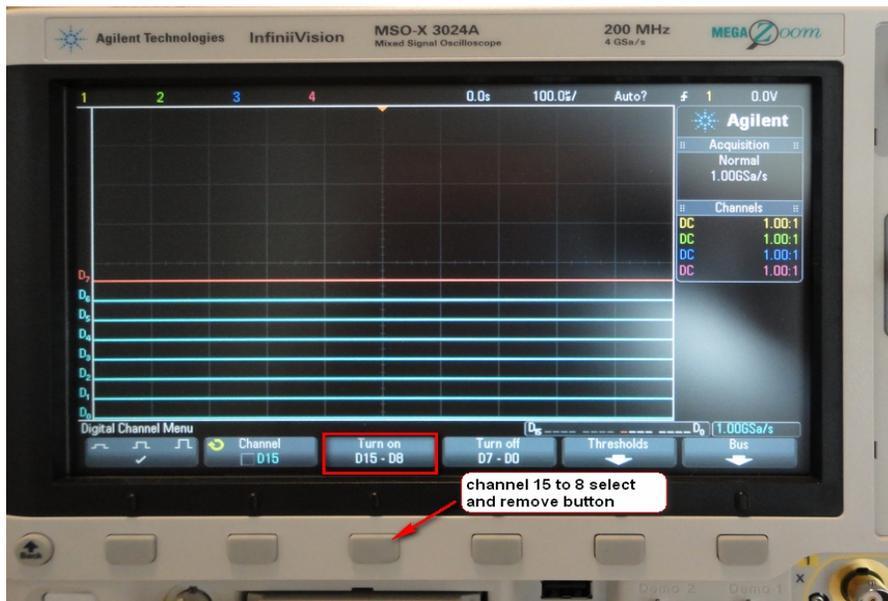

Figure 6 - In this case channels 15 to 8 have been removed

Button 4 -**Channel 8-0** select. This button is used to select or remove channels 8 down to 0 as a group. See figure 7.
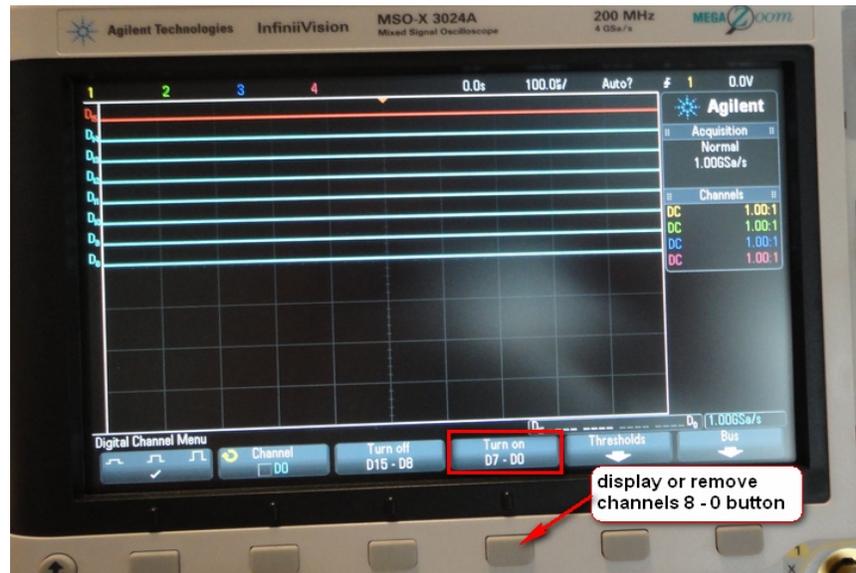

Figure 7- In this case channels 8 -0 have been removed.

Button 5 – **Threshold** select. This allows the user to set different thresholds for the signals. The threshold mode is defined as the voltage range that defines a logic '1' and logic '0'. For this lab we want the threshold to be set to TTL. To ensure this do the following. Press **button 5**. A sub menu will appear. Make sure **button 1** (D15-D8) and **button3** (D7-D0) of the sub menu are set to TTL. If need be use the **select** knob to choose **TTL threshold** mode. See figures 8a, 8b and 8c.
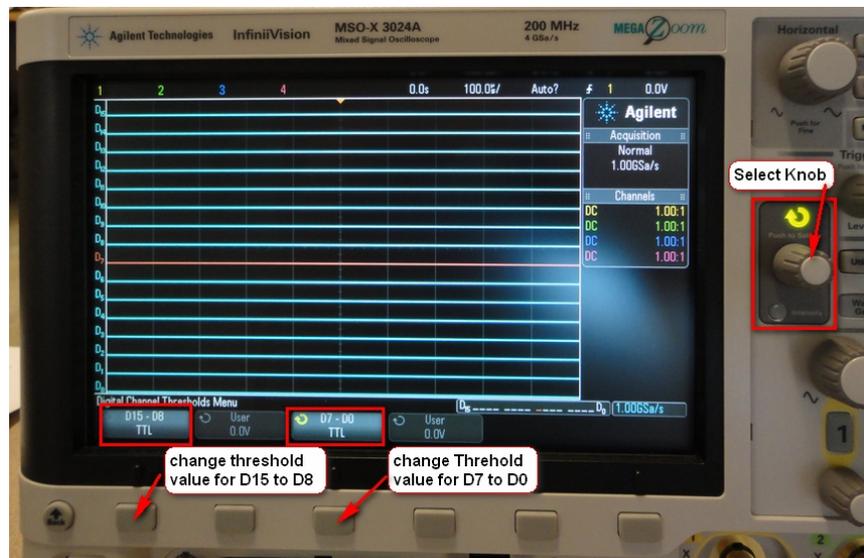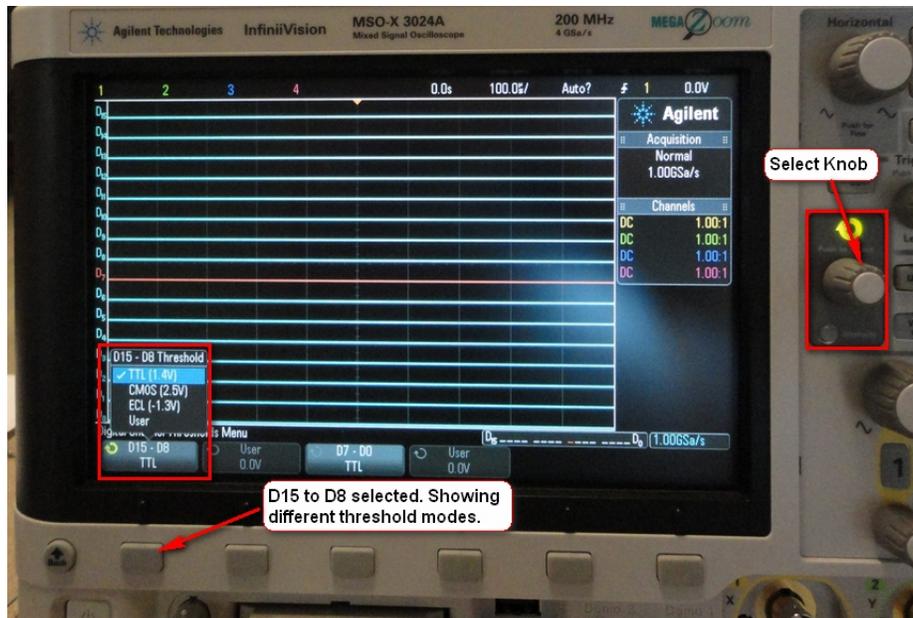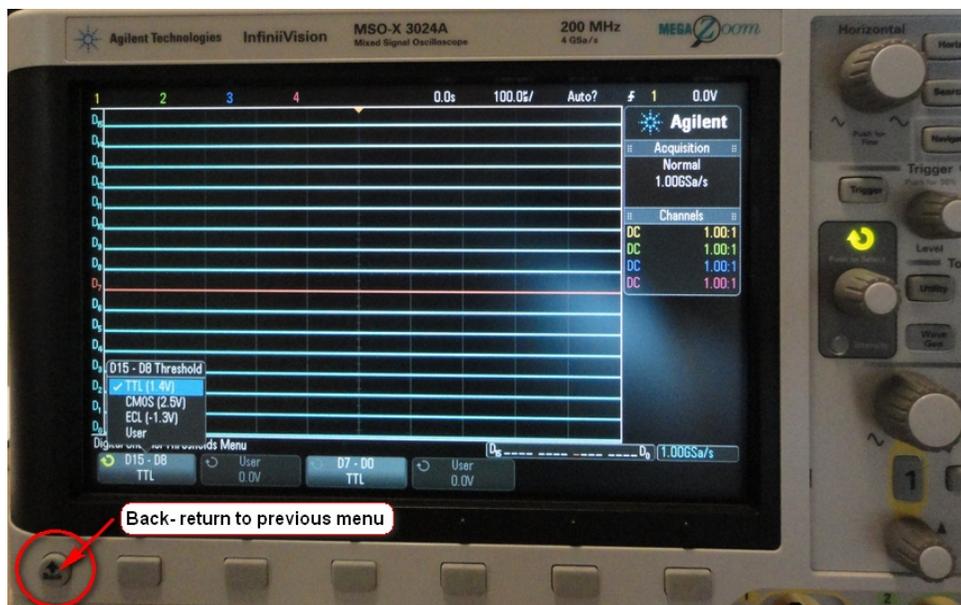

Figure 8a

Figure 8b

Figure 8c

 Press the **back** button to get to the previous menu. See figure 8c for the location of this button.

Button 6- Bus is used for creating a bus. For the purpose of this lab we will ignore this menu. If you want further information, go to the instruction manual found on the DESL home page www-ug.eecg.utoronto.ca/msl. Select Equipment>Scopes. Open the PDF manual for the MSO-X-3024A. Page 27 has a tutorial that explains when to use a bus and how to create a bus.

Before continuing follow these instructions;

Press **the Digital channel select** button as shown in figure 9a. Remove Channels 15 to 8 and set the scale to large. The display should look like figure 9a.
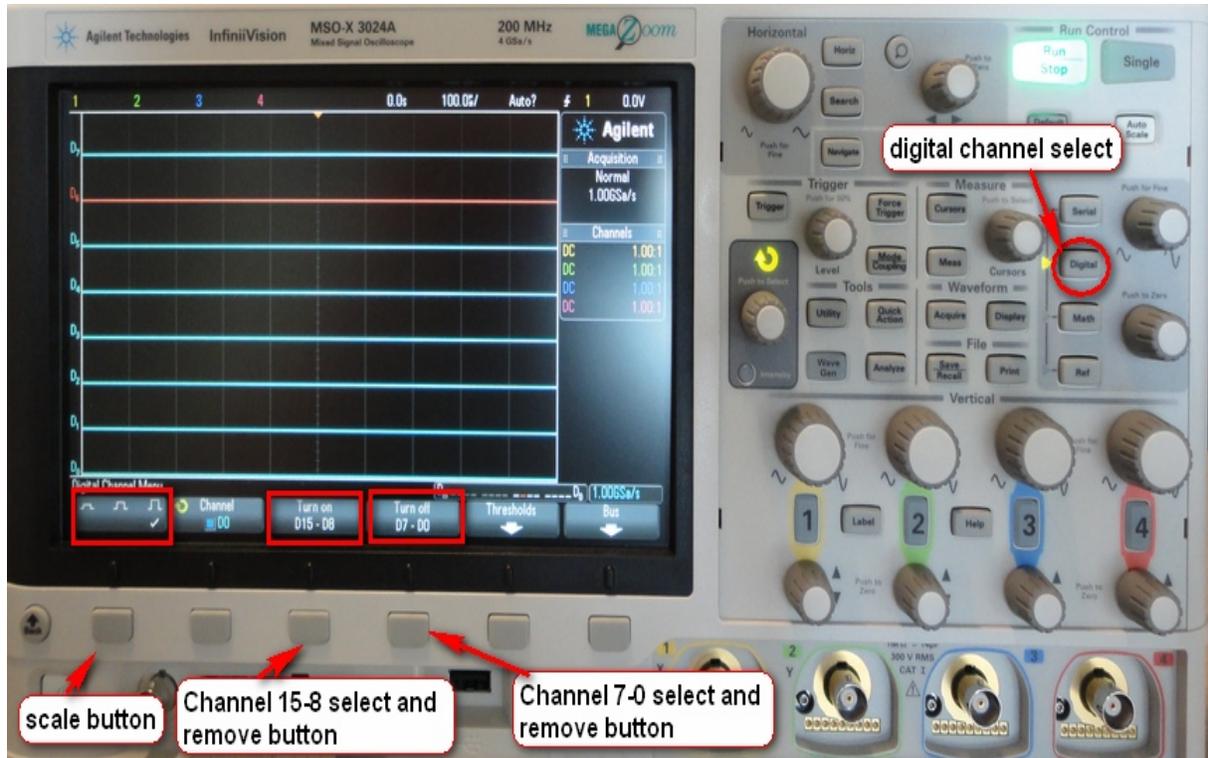

Figure 9a

How to select and move digital channels around

Rotate the **digital channel select** knob. See Figure 9b for the location of this knob. You will notice that as you rotate the knob the selected digital channel will be highlighted RED. To move the location of the channel use the **move channel** knob. See figure 9b for the location of this knob. Note that as you move the knob, channels may share the same location on the display. In Figure 9b Channel 4 and 5 share the same location on the display. You can use the channel **select** knob to select either of these channels. Then you can use the **move** knob to move it to any location on the display.
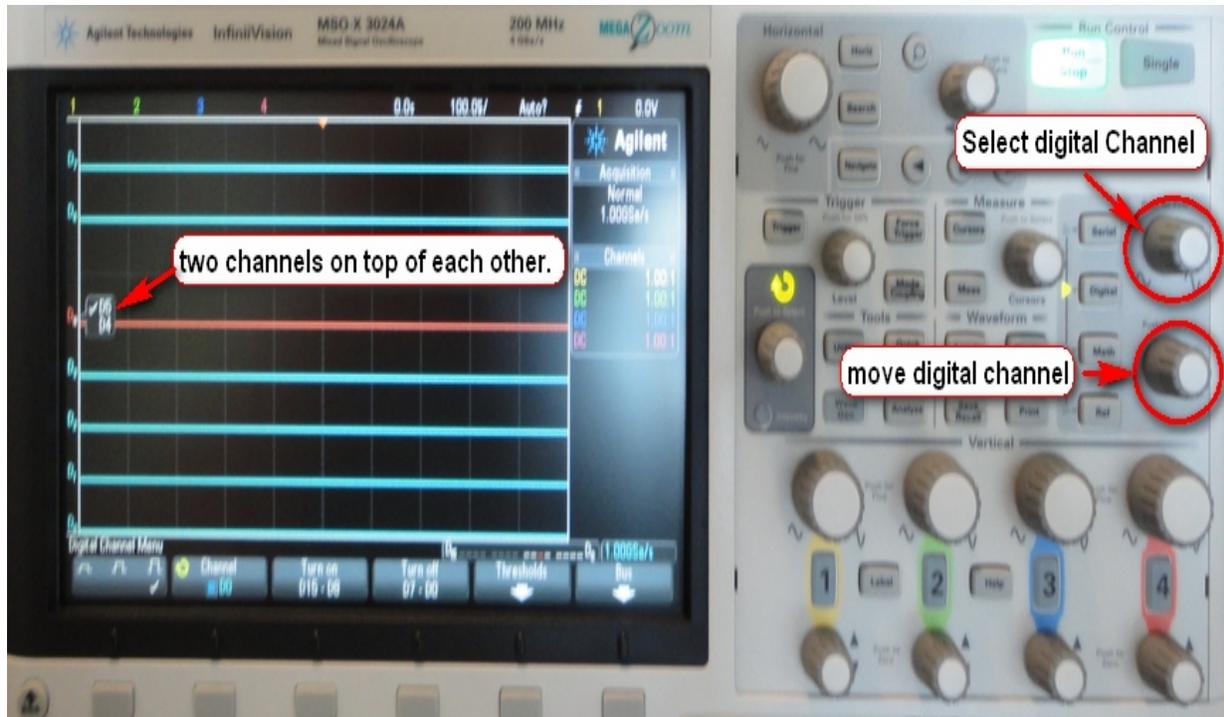
Figure 9b

Output your signals to an output pin

In order to view your signals using the MSO you will need to output the signal to one of the output pins on the JP1 port shown in figure 10. Note that pin 1 starts in the top right corner and the pin numbers increment from right to left followed by top to bottom as shown in figure 11. This will be further explained as we got through both example cases using a BDF file and a Verilog module case.
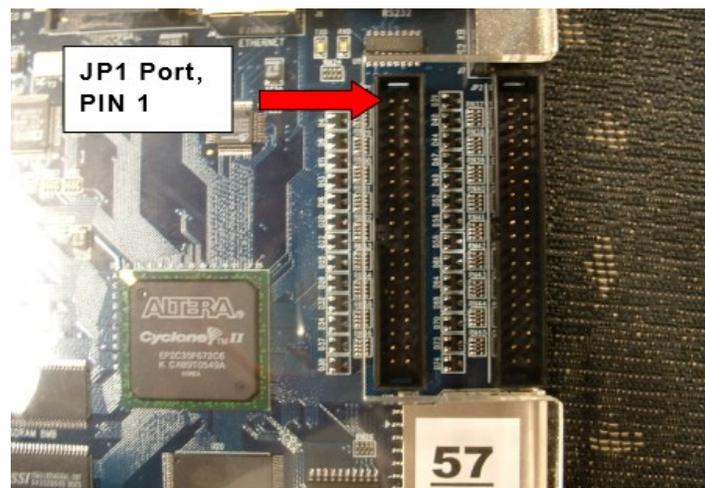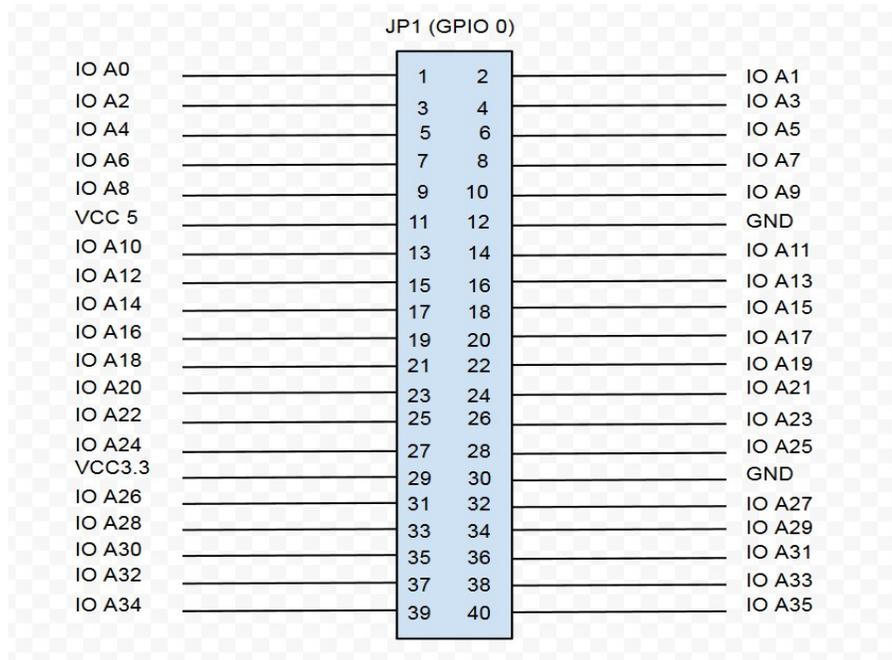

Figure 10- JP1 port (left side on DE2 board.

Figure 11- pin numbers for the JP1 port.

Schematic BDF

Consider the design shown in Figure 12. This is a basic design consisting of 6 inputs (clock, data_ready, data[3..0]), 8 outputs (data_request, a-g), and 5 internal signals (enable, reged[3..0]).
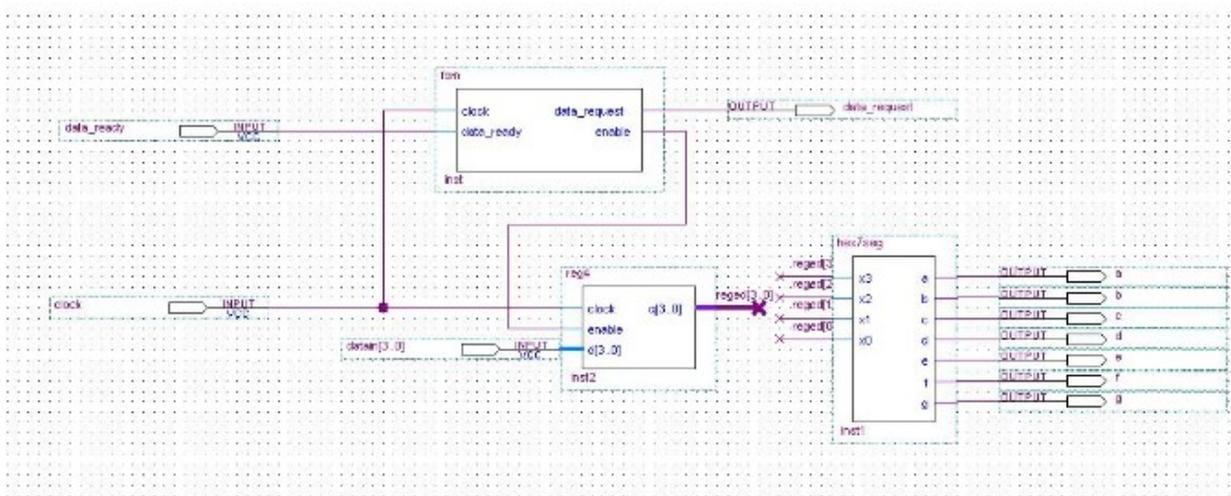

Figure 12 Example design in Schematic format(BDF)

To view the clock we will need to create an output pin, and connect the clock signal to the output pin as shown in figure 13. Here we created an output pin called "clock view" and connected it to the input "clock.
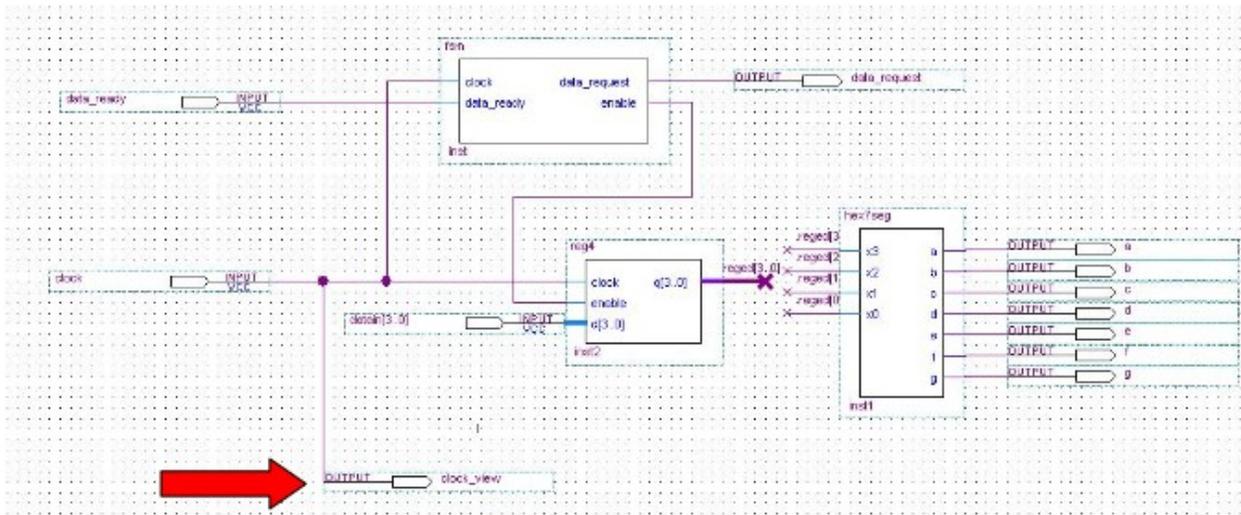
Figure 13 – Output the clock input signal

Following this we will assign the output pins to one of the pins on the JP1 port through the Quartus assignment editor. For example if we want to assign "clock_view" to PIN 1 of the JP1 port, we will assign it PIN_25. The Appendix list found in the main document has all the pin numbers for JP1 port at the back page of the manual..

If you want to view more internal signals and other inputs, you can simply create more output pins as illustrated in figure 14.
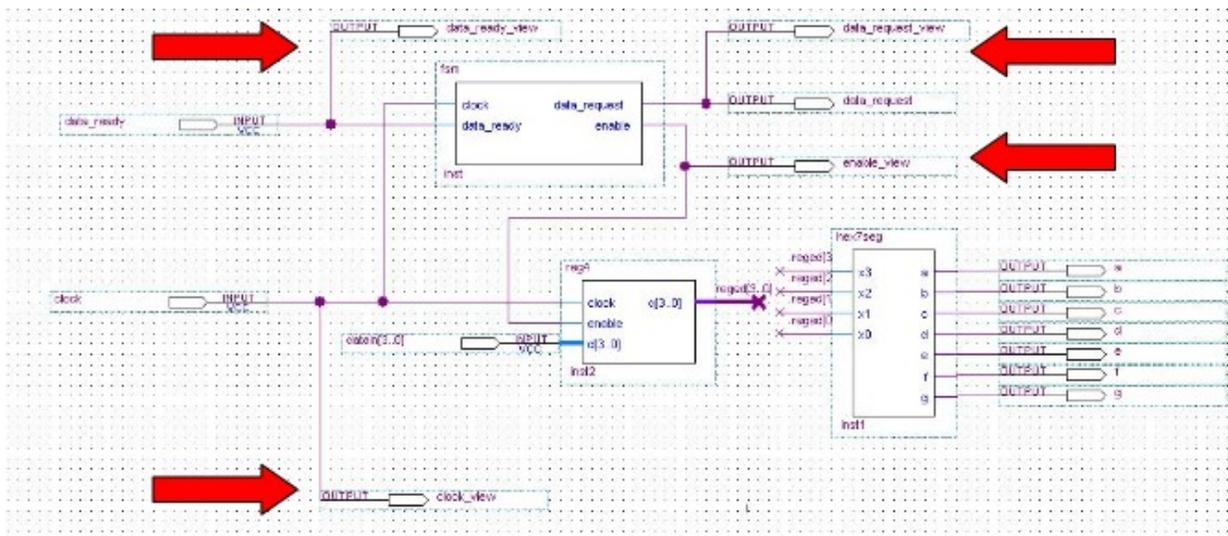

Figure 14- Illustration of viewing several signals on the schematic.

Verilog-To output the pins in a Verilog design, you will need to create an output wire in your port list, and then assign the signal of interest to the new output wire. For example, consider the module

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shown in figure 15. To view the clock, you will need to create a new output wire called "clock_view" and assign the clock input to signal "clock_view" as highlighted in figure 16

```
module top(clock, data_ready, data_request, a, b, c, d, e, f, g, data)

input clock;
input data_ready;

output data_request;
output a, b, c, d, e, f, g;
input [3:0] data;

wire internal_enable;
wire [3:0] internal_regout;

fsm inst( .data_ready(data_ready),
          .clock(clock),
          .enable(internal_enable),
          .data_request(data_request) );

reg4 inst2( .clock(clock),
            .enable(internal_enable),
            .d(data),
            .q(internal_regout) );

hex7seg inst1( .x3(internal_regout[3]),
               .x2(internal_regout[2]),
               .x1(internal_regout[1]),
               .x0(internal_regout[0]),

.a(a), .b(b), .c(c), .d(d), .e(e), .f(f), .g(g) );

endmodule
```

Figure 15 – Verilog module, equivalent to the schematic shown in figure 12.

```
Module

top(clock, data_ready, data_request, a, b, c, d, e, f, g, data, clock_view)

input clock;
input data_ready;

output data_request;
output clock_view;
output a, b, c, d, e, f, g;
input [3:0] data;

wire internal_enable;
wire[3:0] internal_regout;
assign clock_view = clock;

fsm inst( .data_ready(data_ready),
          .clock(clock),
          .enable(internal_enable),
          .data_request(data_request) );

reg4 inst2( .clock(clock),
            .enable(internal_enable),
```

```
               .d(data),
               .q(internal_regout) );

hex7seg inst1( .x3(internal_regout[3]),
               .x2(internal_regout[2]),
               .x1(internal_regout[1]),
               .x0(internal_regout[0]),
               .a(a), .b(b), .c(c), .d(d), .e(e), .f(f), .g(g) );

endmodule
```

Figure 16 – Verilog module to view "clock" with "clock_view" equivalent to the schematic in Figure 13.

Connect your probe leads

The last thing you will need to do is physically attach your probes to the appropriate output pins. Each probe is identified by a number labelled at the end of each probe lead, as illustrated in Figure 17a this corresponds to the signal shown in Figure 17b highlighted in RED.
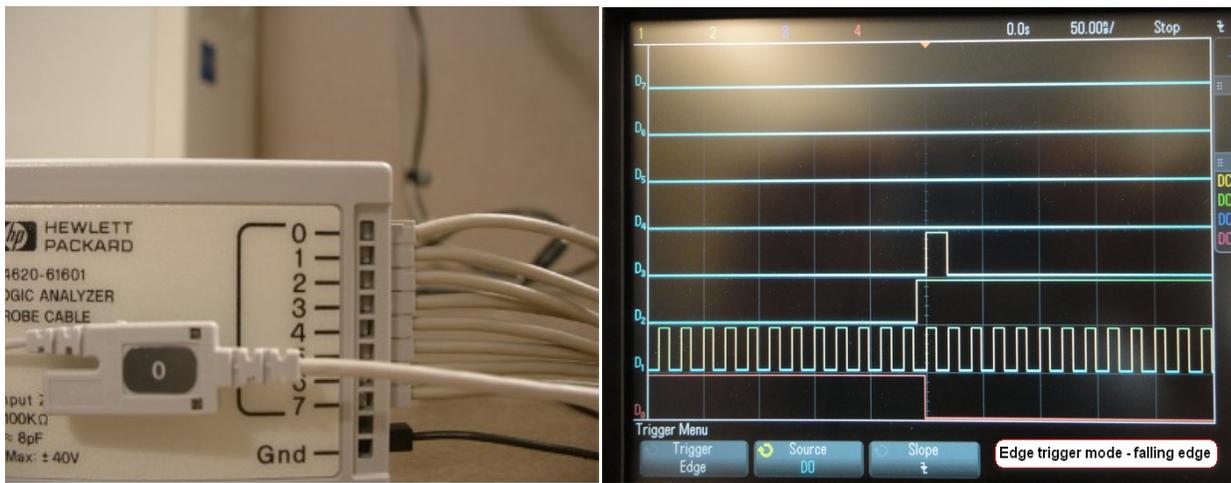
(a)Probe label for probe lead 0   (b) highlighting signal 0 (RED)

Figure 17 Illustration of probes labels (a) and their correspondence to the screen (b).

After you identify which probe leads you want to use, you need to attach the probe heads to your output pins as illustrated in Figure 18.
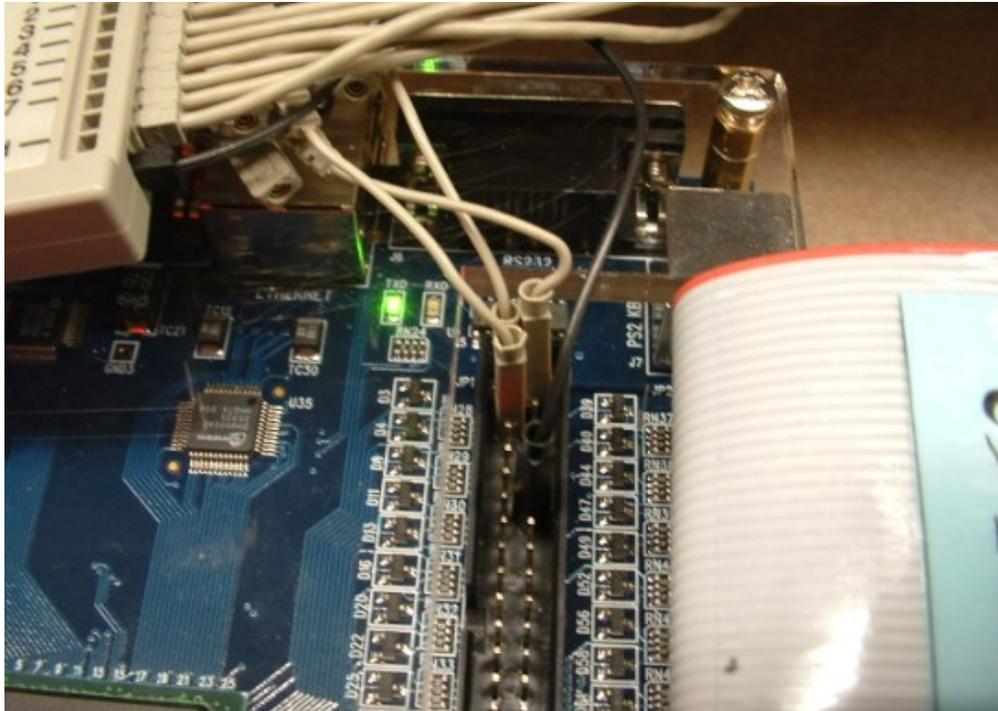
Figure 18 – connecting your probe leads to the JP1 port.

You will need to attach your ground to the ground on the JP1 port. The ground wire is the black wire on the logic probes. This should be attached to pin 12 on the JP1 port. This is highlighted in Figure 19. If you use all 15 channels (both probes) at once, you can connect the second black wire to the pin 30 on JP1.
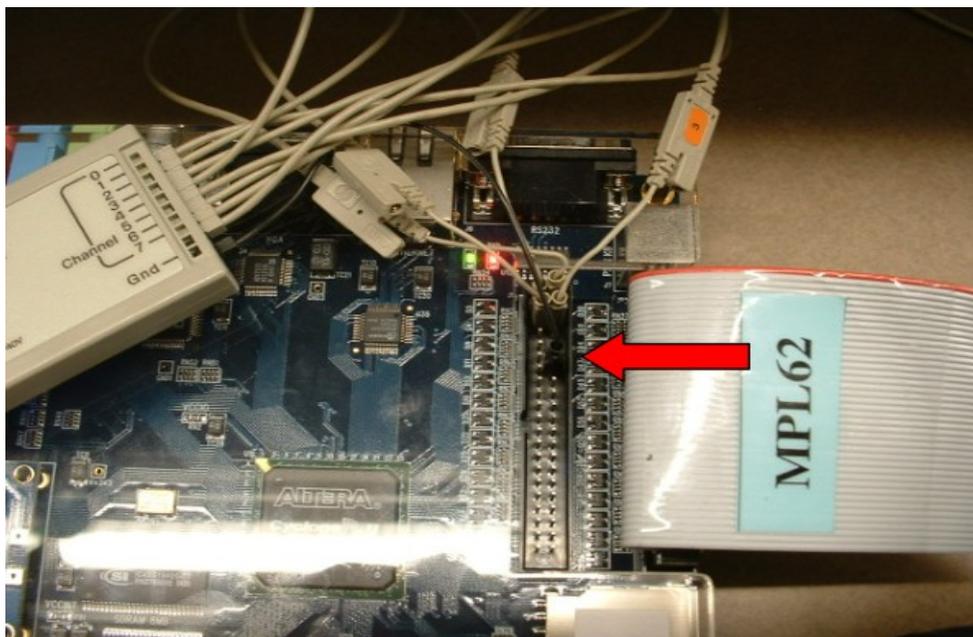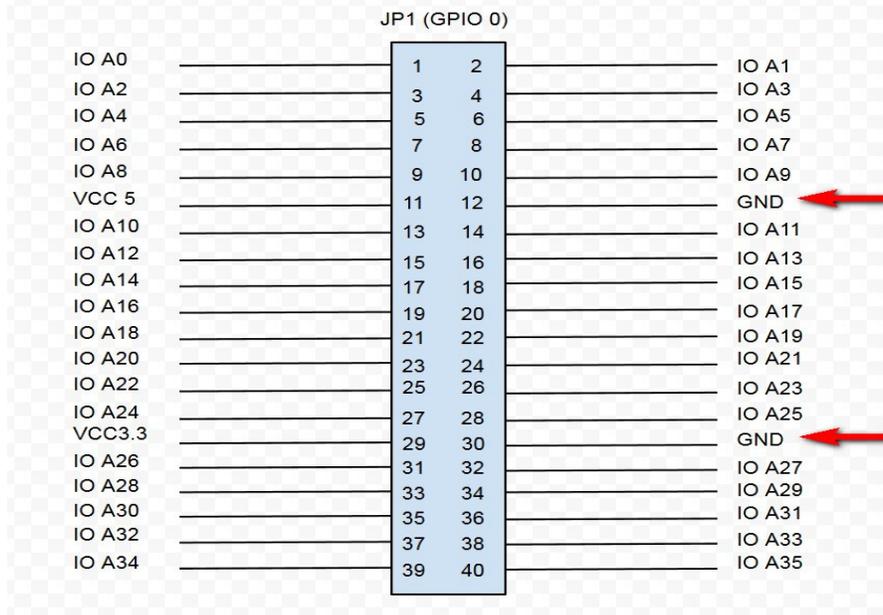

Figure 19 – ground pin location

Figure 20- Illustration of logic probe attached, with ground highlighted.

Setting up a Trigger Event

Often it is necessary to capture a specific pattern on the MSO and freeze that moment in time. This is important during debugging to check the behaviour of your signals during a specific instance in time. Freezing the display at a specific event is possible using your MSO through trigger events.

To setup a trigger event you will need to

- Specify the correct mode for the MSO.
- Set your trigger source.
- Specify the input pattern the trigger will look for.

Setup the Trigger Mode

To change the trigger mode do the following

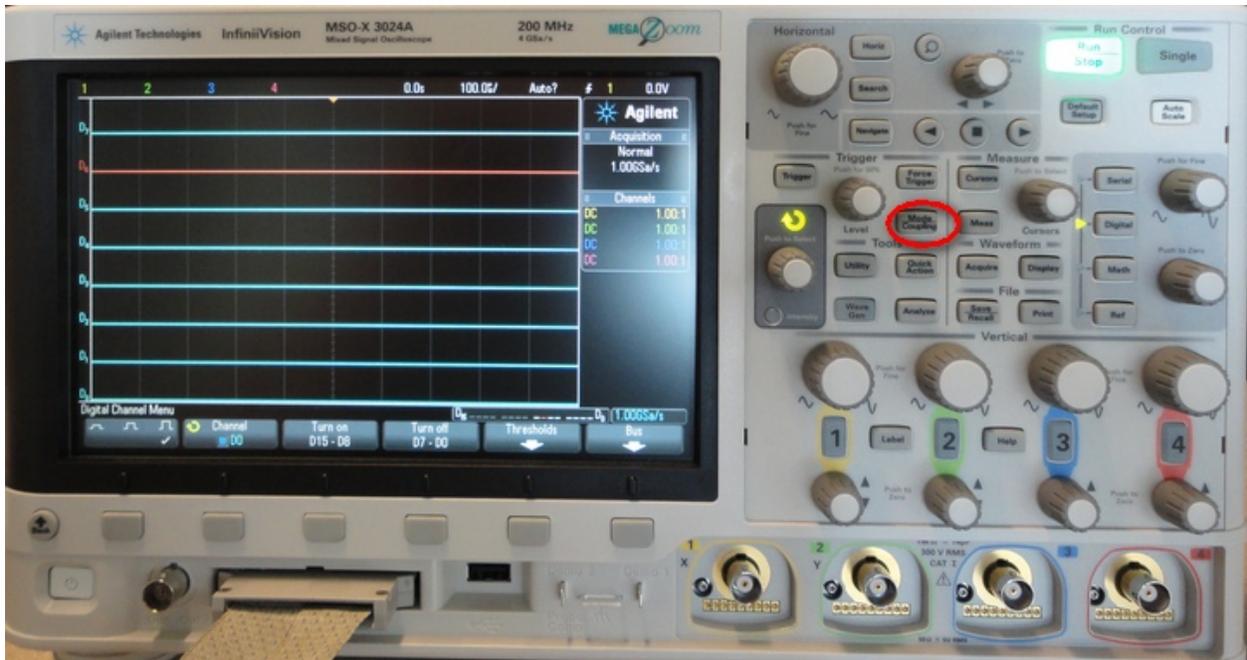Press the **mode/couple** button. See Figure 21 for location.

Figure 21 shows location on panel of mode/couple button.

This will bring up a sub menu on the display screen. Press button 1, see figure 22 for the location. This will give you the different mode options. Using the **select** knob rotate till you have highlighted **normal** mode. Press **select** knob, this select **normal** mode triggering. Make sure **coupling** button 2 is set to **DC.** This is because we are working with digital circuitry. Both **Noise Reg** Button 3 and **HF Request** Button 4 should **not** be highlighted **blue**. **Hold off** button 5 should be set to **40.0ns**. These should be the default settings.
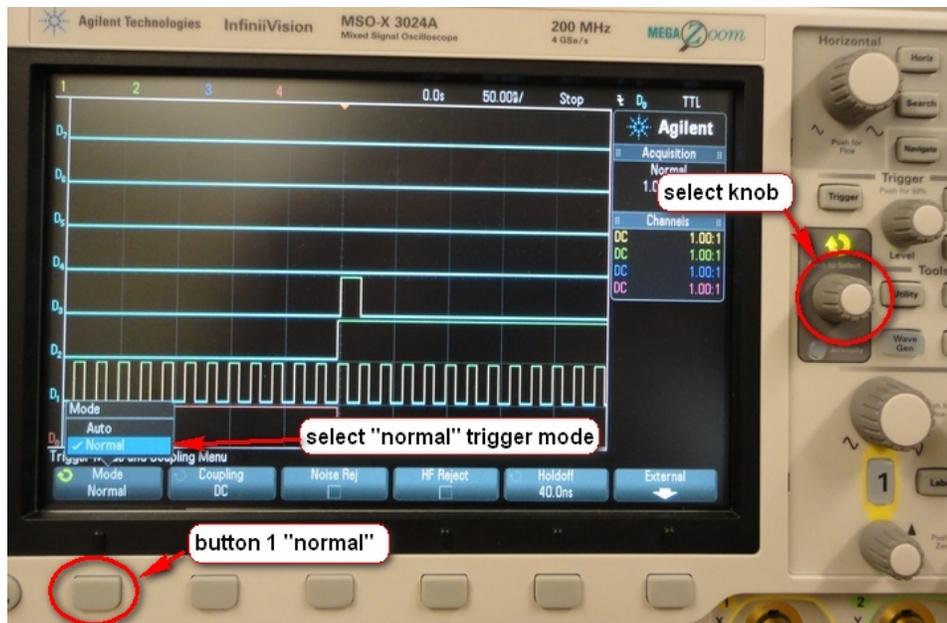
Figure 22

How to Setup Trigger Source

The trigger source is the signal that will be monitored for the trigger event. To setup the trigger source press the **trigger** button as shown in figure 23.
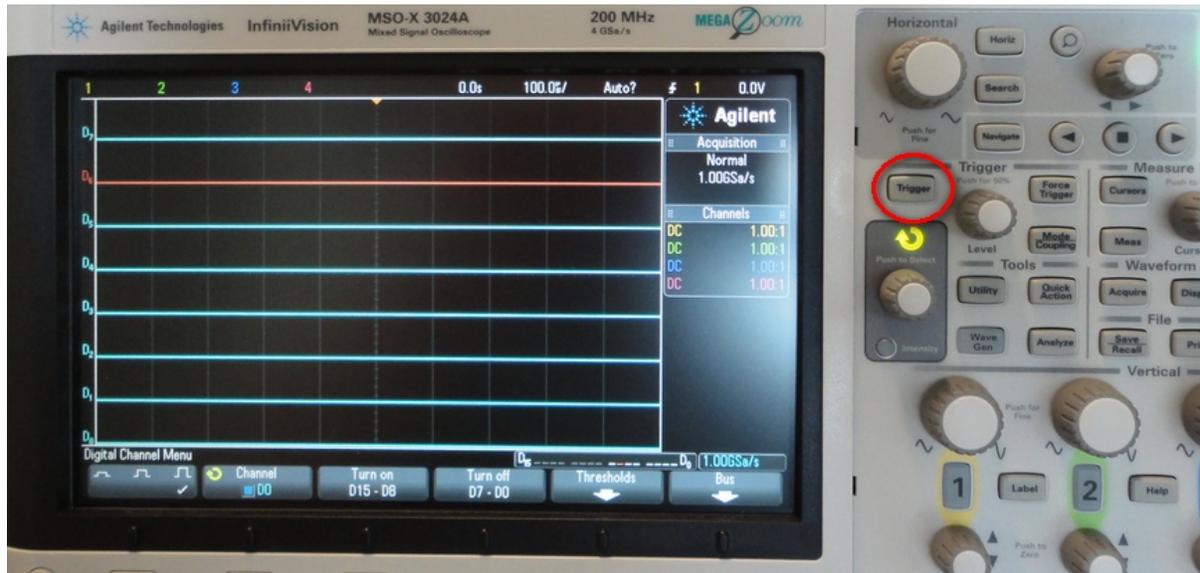

Figure 23

This will bring up a sub menu for setting up all the trigger options. For this example we will be using **D0** as the trigger source and we will be using **edge triggering** (**falling edge**). Press the **trigger** mode button. See Figure 24a. Note the many different trigger modes that there are.
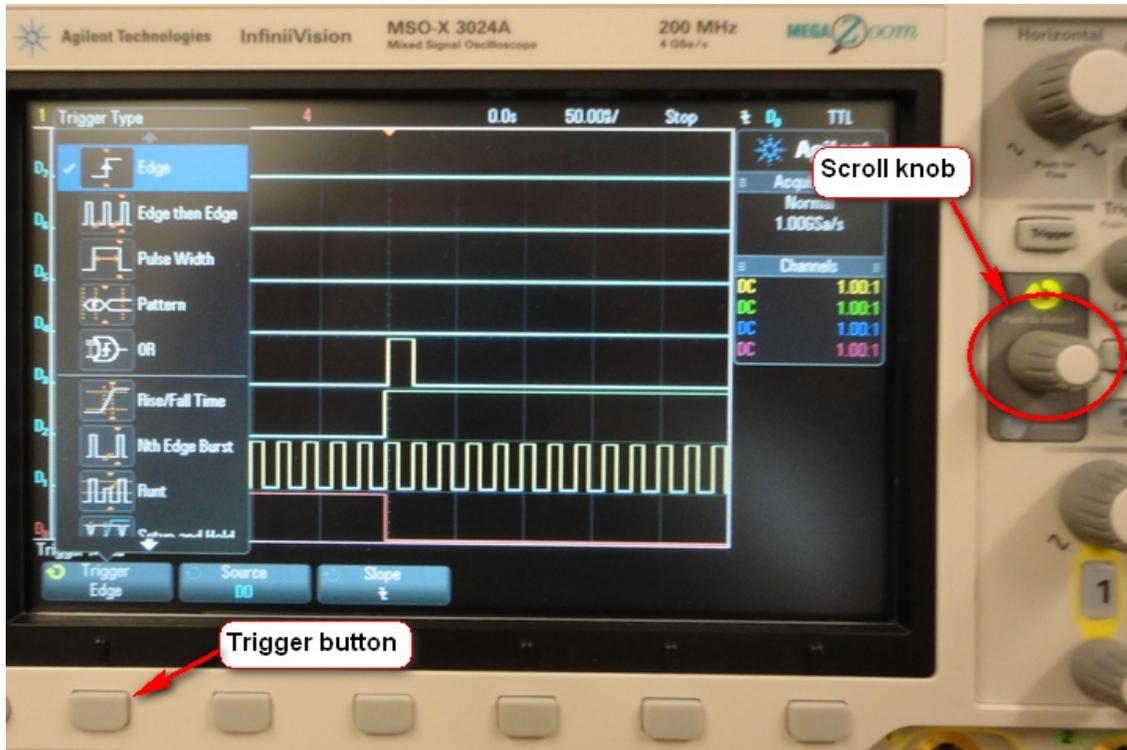
Figure 24a Press Trigger button and use **select** knob choose **edge.** Press **select** knob.

Next press the **source** button and use the **select** knob to select D0. Press **select** knob, see Figure 24b.
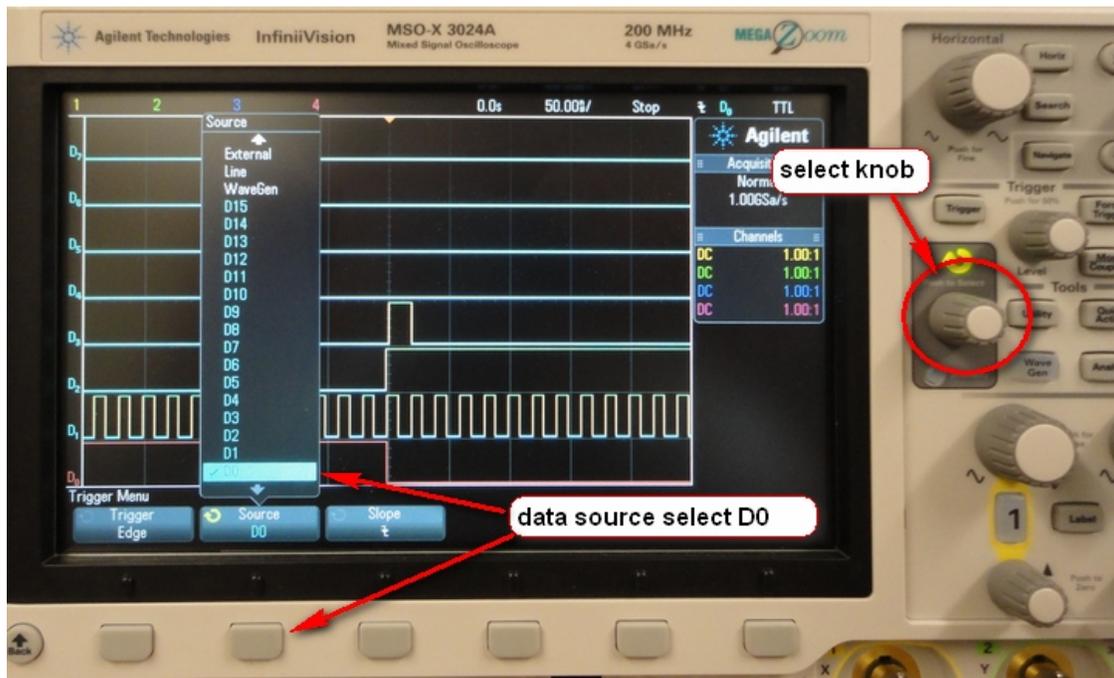

Figure 24b- press data source button and select D0

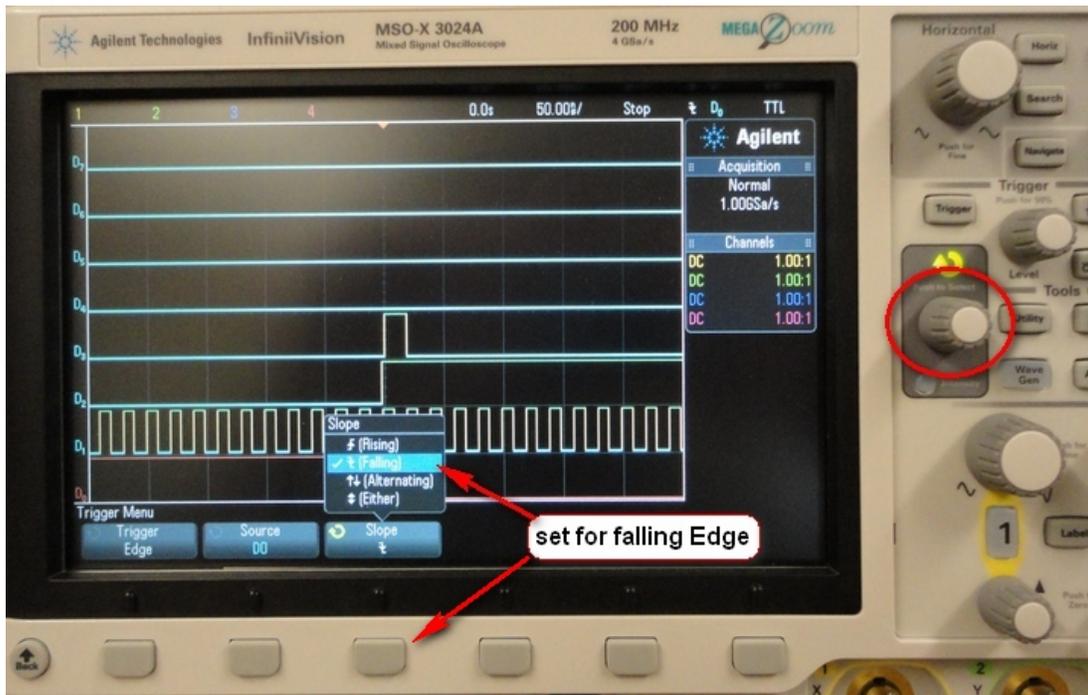Next press the **slope** button and use the **select** knob to select **falling edge**. See figure 24c.

Figure 24c- press **slope** button and select **falling edge**

Now the trigger source has been set up. Now we are ready to capture a trigger event. Press the **Single** button. The **Single** button will be highlighted **yellow**. It will stay yellow until the trigger event we have programmed into the MSO has been fulfilled. Note that no signals appear on the display. See Figure 25.
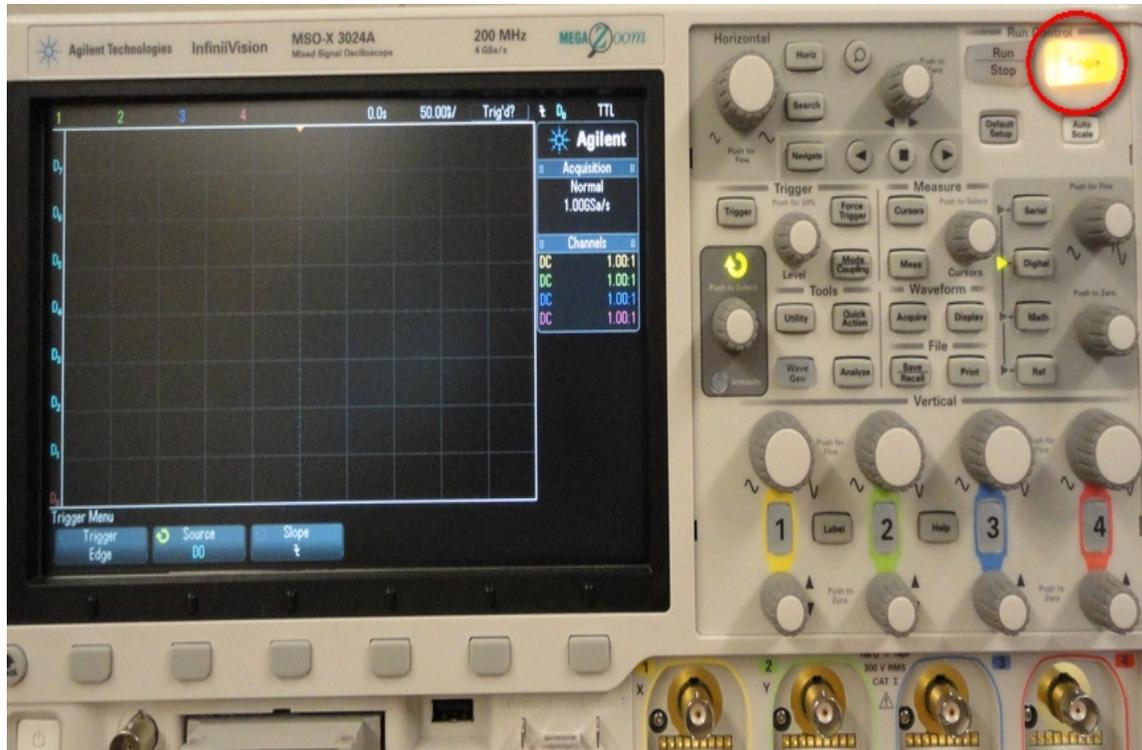
Figure 25- waiting for trigger event to happen

Once the trigger event has occurred the stop button becomes highlighted red and all the data signals are displayed on the screen. In this case we had programmed edge trigger falling edge on D0. See figure 26.
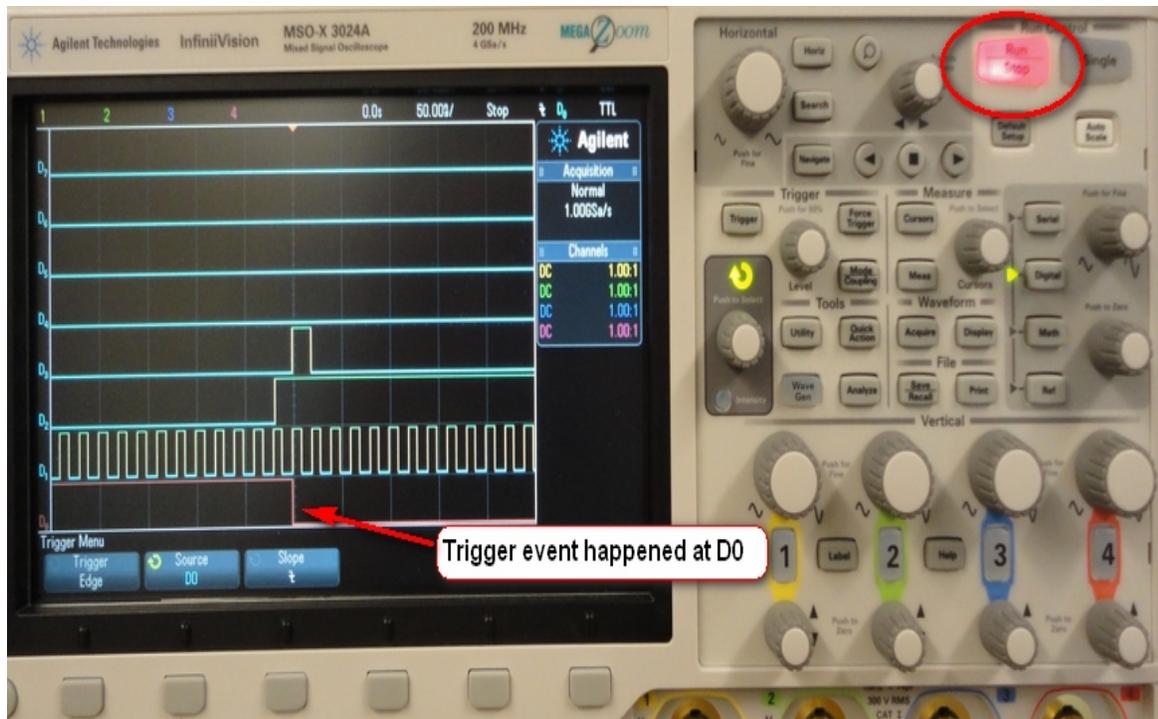
Figure 26- trigger event has happen at D0

There are many different trigger modes on the Agilent MSO-X-3024. Edge triggering is one of the simplest modes. Depending on the complexity of the design more sophisticated trigger modes may be required. For more details on the different trigger modes and tutorials see the manual found on the DESL web site www-ug.utoronto.ca/msl. Select Equipment>Scopes. Select the manual for the MSO-X-3024. There are several tutorials on how to set them up and trigger.